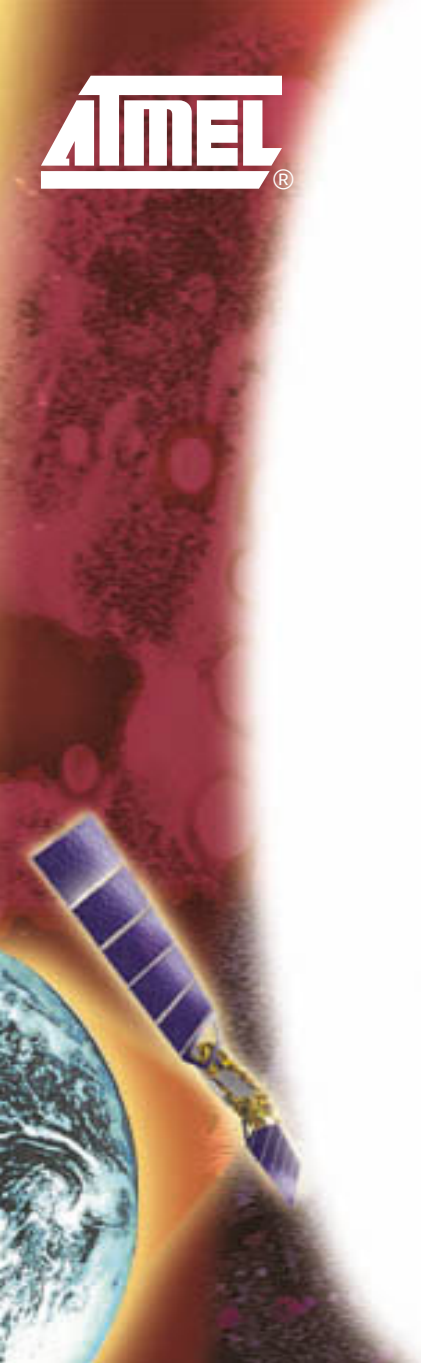

ATC18RHA - Offering Overview

MPW Workshop - ESTEC

June 17th, 2004

Summary

- ATC18RHA Features
- Standard Cell Library
- I/Os Libraries
- Memory Libraries
- Die sizes
- Assembly and Packages
- ATC18RHA availability

ATC18RHA Features

- **Technology**
  - 0.18µm CMOS Rad Hard technology
  - 5 metal layers
  - 1.8V power supply for the core
  - 1.8V and 3.3V power supply for the periphery
- **Libraries**
  - Standard Logic and IO Cells Libraries
  - Memory libraries
  - PLL (480MHz)
- **Space standards**
  - High Reliability
  - Radiation
    - TID better than 200Krads
    - SEL better than 70MeV.cm²/mg

Standard Cell library

- Buffers and Gates
- Multiplexers
- Standard and SEU Hardened Flip-flops
- Standard and SEU Hardened Scan Flip-flops
- Latches
- Adders and Subtractors

I/Os libraries

- 2 libraries
  - IO18 : 1.65 to 1.95V
  - IO33 : 3.0V to 3.6V
- Buffer types
  - Bidirectional
  - Tristate Output
  - Output Only
  - Input Only (Inverting,Non-Inverting,Schmitt Trigger)
- Additional buffers of IO33 library
  - 3.3V PCI Bidirectional, Tristate Output and Output Only
  - LVDS Transmitter and Receiver differential (based on the ANSI/TIA/EIA-644 Standard)
  - LVPECL Receiver differential

I/Os libraries

- **IO33 and IO18 buffers are Cold Sparing**
  - **When VCCB is “off” these pads have a negligible leakage current**
- **Standard IO33 buffers are tolerant (PCI,LVDS,LVPECL excepted)**
  - **When the pad is configured as an input, and VCCB is < 3.3V (ex 1.8V), the external signal can go up to 3.3V (max 3.6V) with negligible leakage current**
- **An IO33 standard buffer with VCCB=1.8V can also be used as a 1.8V Compliant Output with degraded IOL,IOH and timing performances**

Memory libraries

- Compiled memories
  - VIRAGE compilers
    - SRAM (32kx16)
    - DPRAM (8kx32)
    - TP Register File (1kx16)
  - Synchronous only
  - EDAC VHDL
- Synthesized memories
  - Genesys Atmel software
    - RAM (4k)
    - TPRAM (4k)
    - DPRAM (2k)
  - Asynchronous
  - SEU hardened cells used

Die sizes

- 95µm pad pitch and pad width, except
  - LVDS transmitter
    - width= 3x95µm and pitch=190µm
  - LVDS Receiver and LVPECL Receiver
    - width=2x95µm and pitch=95µm
- Predefined die sizes
  - To allow re use of existing MH1RT packages
  - To ease the SMPW management

Predefined die sizes

	Equivalent MH1 matrix size	Size (mm^2)	Program-mable pads	Buffer Power supply pads	Typical Nbr of Gates
ATC18RHA95_216	NA	6.19x6.19	216	8	1M
ATC18RHA95_324	MH1099E	8.76x8.76	324	8	2.2M
ATC18RHA95_404	MH1156E	10.66x10.66	404	8	3.5M
ATC18RHA95_504	MH1242E	13.03x13.03	504	8	5.5M

Preferred Hermetic Multi-layer Packages

SMD 5962-....		Matrix Variant					
SMD / Package Variant		Number of leads	Marketing Code	ATC18RHA95_216	ATC18RHA95_324	ATC18RHA95_404	ATC18RHA95_504
MQFPF		T352	YC		U88N (*)	U85N (*)	U80N (*)
		256	KZ		U89N (*)	U90N (*)	U76N (*)
		196	K9	X(*)	U92N		
		160		X(*)			
MCGA		625 (**)	2D				EF401 (*)
		472	2C			H06N (*)	H05N (*)
		349	2E		H04N (*)	EF378 (*)	EF379(*)
Die		Die	0	0	0	0	0

(*) 4 decks package (**) fine pitch 1mm

Double pad ring

- Pad pitch 95µm (ceramic package limitation)
- Inner ring for core power supply
- Outer ring for buffer power supply and IOs
- ATC18RHA95_504 ‘matrix’
- Prototype level only

- Future development
  - Double pad ring for FM and any ‘matrix’
  - Flip chip assembly

Development status

- **Beta Design Kit available since end of March 2004**
  - **2 CDROMs : ASIC Design Kit and SIGMA Design Kit**
  - **NDA requested for the SIGMA Design Kit**
- **Beta design**
  - **ATC18RHA95_504, MCGA472, double pad ring**
  - **Design Review, mid of July**
  - **1st samples in November**
- **Final design kit to be released end of 2004**
  - **Results of V34 and V35 silicon (characterization and radiation)**
  - **On DVD**